JSPM's
Bhivarabai Sawant Institute of Technology and Research
Wagholi, Pune-412207

Department of Electronics and Telecommunication Engineering

A report on "A webinar on "VLSI Design using Verilog HDL"

Objective	**To create awareness among the students & faculty members about VLSI design technology|: CPLD & FPGA , Design of SOC ,Study of verilog, Data types , coding in VLSI.**
Date of Conduction	**1st Feb 2019**
Speaker	**Mr P R Sivakumar, CEO Maven Silicon.**
Timing	**10 am to 1 pm**
Coordinator	**Prof. P. R. Shah, Prof. V. G. Puranik & Dr. Y. S. Angal**
Students & Faculties Participated	**70 students & 10 faculties**

Prof. P. R. Shah, Coordinator given the importance & flow of webinar.

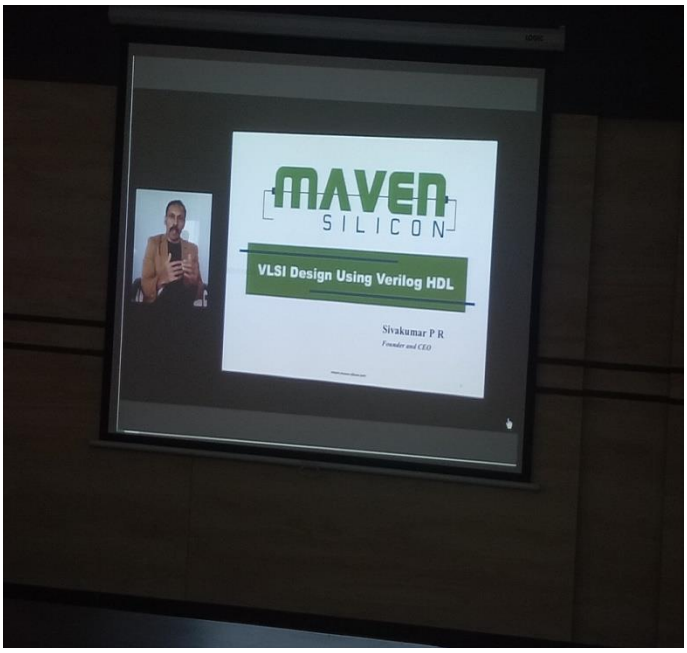

Photo1: LHS – Prof. P. R. Shah, introducing the contents of webinar
RHS – Mr P R Sivakumar, CEO Maven Silicon, started with session

The session of the webinar was on "VLSI design & Designing of SOC" started at 10.00 am. **Mr P R Sivakumar, CEO Maven Silicon,** provided best knowledge regarding VLSI design and Designing of SOC. He provided valuable information of Verilog with its features, coding, applications & data types. He had given important information regarding how to debug the code, how to write the code using VHDL.

Photo2: Interaction of Faculties and Students with expert in webinar

Photo3: Group photo of all participants after successful completion of webinar

Expected Outcome: After successful webinar on "VLSI Design using Verilog HDL", students and faculties get acquainted with basic knowledge of VHDL programming and will be able to program any application using VHDL.

Prof. P. R. Shah, Prof. V. G. Puanik & Dr. Y. S. Angal
Coordinators

Dr. Y.S.Angal
H.O.D.(E&TC)

Dr. T.K.Nagaraj
Principal